**In the Specification:**

Please amend paragraph 33 to read as follows:

**[0033]** When a back-end ASIC receives the slave sync signal, the synchronization control logic recognizes the signal and carries out a procedure that aligns internal ports. This procedure may be referred to as "port-to-port synchronization". Port-to-port synchronization aligns each internal port by adding or subtracting, if necessary, a delay to the FIFO receive buffers of an ASIC that received a slave sync signal. This delay is based upon the value of the word counter associated with an ASIC and the received word counter value in the slave sync signal.

Please amend paragraph 36 to read as follows:

**[0036]** The additional cycles of latency during port-to-port synchronization preferably are incorporated in a FIFO receive buffer by setting one or more control bits in the associated synchronization control logic. The control bits preferably determine the wait time (in cycles) a piece of data is held in the FIFO receive data ~~slot~~ buffer before being received from the FIFO. The synchronization control logic coupled to an ASIC is responsible for setting the control bits to the appropriate values.

Please amend paragraph 39 to read as follows:

**[0039]** Referring now to Figure 7, a ~~block diagram~~flow chart of the exemplary synchronization procedure is shown in accordance with preferred embodiments. The synchronization procedure starts with synchronization event, such as a power-on procedure or a reset. The ASIC designated as the master ASIC transmits a master sync signal on all of its ports (block 202). Any ASIC that receives the master sync signal (block 204) sets its word counter to the value contained in the master sync signal plus the synchronization advance value, as previously discussed (block 206). In addition, any ASIC that receives the master sync signal sends a first slave sync signal on all of its ports (block 208). An ASIC, upon receiving the first slave sync signal (block 210), may set its word counter to the value in the latest slave sync signal received and perform port-to-port synchronization, as previously discussed (block 212). A second slave sync signal is sent from all non-master ASIC ports receiving the first slave sync signal (block 214) and this second slave sync signal is received by one or more ASICs (block 216). Upon receiving the second slave sync signal,

port-to-port synchronization is performed on the ports that received the second slave sync signal (block 218), thereby completing the synchronization.

Please amend paragraph 45 as provided below.

**[0045]** In some embodiments, a front-end ASIC may be assigned as the master ASIC. The first synchronization stage may send a master synch from the master front-end ASIC; the second synchronization stage may send a slave sync from one or more back-end ASICs to one or more front-end ASICs; and the third synchronization stage may send a slave sync from one or more front-end ASICs to one or more back-end ASICs.